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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,668	01/30/2004	Yutaka Saeki	NEM-05301	8256

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EXAMINER
SITTA, GRANT

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/768,668	SAEKI, YUTAKA	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-12,25,28 and 29* is/are pending in the application.

4a) Of the above claim(s) *4- 5 and 8-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,6,7,25,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 2, 25, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by DeCaro et al (6,965,360) hereinafter, DeCaro

2. In regards to claim 1, DeCaro teaches a current-drive apparatus for a display panel (abstract, "visual displays" fig. 1 (100)), comprising: a plurality of current-drive circuits (fig. 7 and 11 (710, 720, etc)), each of said plurality of current-drive circuits section including first (fig. 7 input to 200 from 750 in 710) and second (fig. 7 (200) output 716 to 200 of 720) terminals a reference resistor connected between said first and second terminals (fig. 2 (288and 282)) and a reference current generation circuit (fig. 2 (200) "balancing circuit") to produce at least one internal reference current (col. 6, lines 3-15) responding to a voltage generated based on the reference resistor; and

a current source (fig. 7 and 11 (750)), said current source and said plurality of current-drive circuits being connected such that a current flowing through said current source becomes substantially equal to a current flowing through said reference resistor of each (col. 15, lines 18-20) of said current-drive circuits (col. 14-15, lines 64-28), wherein a current flowing through said reference resistor in a first one of said current-

drive circuits flows through said reference resistor in a second one of said current-drive circuits (fig. 7 and 11 (750) and Iref)),

wherein said current drive circuits are coupled in series (fig. 7 710, 720 and 730 are in series) in a manner that said first terminal of a preceding one of said current drive circuits is connected to the second terminal of a succeeding one of said current-drive circuits which is adjacent to the preceding one of said current-drive circuits (first (fig. 7 input to 200 from 750 in 710) and second (fig. 7 (200) output 716 to 200 of 720) terminal which are connected in series, while not directly connected, the first and second terminal are connected to the succeeding current drive circuit) and

wherein at least one of said plurality of current-drive circuits further includes at least one current adjustment resistor (fig. 2 (240 and 242) the matched resistors compensate for current imbalance col. 6, lines 55-58) that operates such that a reference voltage generated across said reference resistor is applied across said at least one current adjustment resistor to generate said at least one internal reference current (col. 6, lines 55-58)..

3. In regards to claim, 25 DeCaro teaches a current-drive system for a display panel (fig. 1 (100)), comprising: first and second power source lines (fig. 2 common electrode line and ground col. 5, lines 54-67); a plurality of current-drive ICs (fig. 7 (710-730)), each of said plurality of current-drive ICs having first and second terminals (fig 7 input and output terminals of 710-730) and having a first resistor connected between said first and second terminals (fig. 2 (288) and 282); and

a current source (fig. 2 (270)) connected to said plurality of current-drive ICs so that said ICs and said current source are connected in cascade (fig. 7 (710, 720, and 730)) with said first and second terminals between first and second power source lines (col. 14-15, lines 64-28).

wherein said ICs are coupled in series (fig. 7 710, 720 and 730) between said first power source line and said current source in such a manner that the second terminal of a preceding one of said ICs is connected to the first terminal of a succeeding one of said ICs (fig. 7 710, 720 and 730 col. 14-15, lines 29)

wherein at least one of said plurality of current-drive ICs produces an internal reference voltage based on a voltage generated across said first resistor (fig. 2 (240 and 242)). and

wherein at least one of said plurality of current-drive ICs further includes a second resistor having a first end coupled to one end of the first resistor and having a second end coupled to the other end of the first resistor. (fig. 2 (240 and 242)). Examiner notes that they are directly connected through 298 and other ends are connected through the common electrode.

4. In regards to claim 29, DeCaro teaches a current-drive apparatus according to claim 1, wherein said current-drive circuit is operable to sum up at least one internal reference current in a desired number and output a desired number of internal reference currents to a display element of said display panel (fig. 2 (260a-260e)). Examiner notes

the total current is the sum of the currents through the individual components, in accordance with Kirchhoff's current law.

5. In regards to claim 30, DeCaro teaches a current drive circuit according to claim 13, wherein said current-drive circuit is operable to sum up said at least one internal reference current in a desired number and output a desired number of internal reference currents (fig. 2 (260a-260e). Examiner notes the total current is the sum of the currents through the individual components, in accordance with Kirchhoff's current law.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 6, 7 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeCaro, in view of Yatabe et. al (US 6,188,395) hereinafter, Yatabe.

9. In regards to claim 6, DeCaro discloses the limitations of the current-drive apparatus according to claim 1.

DeCaro differs from the claimed invention in that DeCaro does not disclose wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a high voltage supply and a plurality of second operational amplifiers, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a low voltage supply, and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal reference current

However, Yatabe teaches a system and method for wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier (fig. 1 2a), provided as a voltage follower (fig. 1 (2a) voltage follower), for outputting a voltage appearing at a terminal of said reference resistor (fig. 1 R8) on the side of a high voltage supply (fig. 1 (VDD)) and a plurality of second operational amplifiers (fig. 1 (2b)), provided as a voltage follower (fig. 1 (2b) voltage follower), for outputting a voltage

appearing at a terminal of said reference resistor on the side of a low voltage supply (fig. 1 VEE), and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal reference current ((fig. 1 R8,R9, R10 and R11 is applied to both terminals col. 7, lines 1-30 of Yatabe).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify DeCaro to include the use of wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a high voltage supply and a plurality of second operational amplifiers, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a low voltage supply, and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal reference current as taught by Yatabe in order to provide a means to reduce the potential difference between the two driving potentials and thus provide a reduction of voltage resistance in the circuit device which causes the production cost and power source circuit to be reduced as as stated in (col.

4, lines 25-47 of Yatabe).

10. In regards to claim 7, DeCaro as modified by Yatabe teaches the current-drive apparatus according to claim 6, wherein said at least one of said plurality of current-drive circuits further includes a reference current part (fig. 1 C5 and C6of Yatabe)) disposed between each of said of current adjustment resistor and said low voltage supply (fig. 1, R8,R9, R10 and R11 and VEEof Yatabe), and is configured so that an output of corresponding one of said plurality of second operational amplifiers is input to said reference current part in order to allow said corresponding one of said at least one internal reference current to flow to said low voltage supply (fig. 1 through OP4 through C4 the smoothing capacitorof Yatabe).

11. In regards to claim 28, DeCaro discloses the limitations of the system as claimed in claims 25, wherein at least one of said plurality of current- drive ICs further includes.

DeCaro differs from the claimed invention in that DeCaro does not disclose a first OP amplifier having an input coupled to a node between said first terminal and said first resistor and an output thereof; a second OP amplifier having an input coupled to a node between said second terminal and said first resistor and an output thereof; and a second resistor coupled between the outputs of said first and second OP amplifiers.

However, Yatabe teaches a system and method for a first OP amplifier having an input coupled to a node between said first terminal and said first resistor and an output

thereof (fig. 1 OP1 and R8); a second OP amplifier having an input coupled to a node between said second terminal and said first resistor and an output thereof; and a second resistor coupled between the outputs of said first and second OP amplifiers (fig. 1 OP2 and R9).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify DeCaro to include the use of a first OP amplifier having an input coupled to a node between said first terminal and said first resistor and an output thereof; a second OP amplifier having an input coupled to a node between said second terminal and said first resistor and an output thereof; and a second resistor coupled between the outputs of said first and second OP amplifiers as taught by Yatabe in order to provide a means to reduce the potential difference between the two driving potentials and thus provide a reduction of voltage resistance in the circuit device which causes the production cost and power source circuit to be reduced as stated in (col. 4, lines 25-47 of Yatabe).

Response to Arguments

1. Applicant's arguments filed 05/05/2009 have been fully considered but they are not persuasive.

Examiner notes that claims 4,5 and 8-12 are maintained and currently are in withdrawn status, but pursuant to MPEP 821.04 (B) upon the allowance of a base generic claim, these claims should be rejoined and would be considered fully examined for patentability under 37 CFR 1.104.

2. Applincant submits that the reference resistor and the current adjustment resistor recited by Applicant are not the same resistor and that DeCaro does not teach features recited by Applicant involving a reference resistor (or first resistor) and a current adjustment resistors (or second resistor). Examiner respectfully disagrees. In regards to the current rejection DeCaro states:

> "The following paragraphs provide a description of the operation of the balancing circuit 200. As described above, each of the resistors 260, 282, 284, 286 and 288 are connected to the common electrical connection 280, yielding a common voltage potential at the connection 280. The common voltage potential at the common connection 280 and the connection of transistors 230, 232, 234 and 236 to the group driver circuit 120, as described above, results in a closely matching current flowing through each of the column transistors 214." (col. 6, lines 41-50)

DeCaro uses balancing circuits (fig. 7 (200) and fig. 2 (200)) to result in a closely matched current through the columns (col. 6, lines 41-50). The balancing circuit uses resistors 240, 242, 284, and 288 resulting in the closely matched current. The resistors 282, 288 are in series with resistors 240 and 242.

> "The balancing circuit 200 further comprises two closely matched and closely spaced resistors 240 and 242, each having an upper end (in relation to FIG. 2) connected to the drain terminals 296 and 272 of the source transistors 230 and 234, respectively. In one embodiment, the two resistors 240 and 242 are closely matched if the tolerance variance between them allows the precision of current matching desired to be achieved" (col. 6, lines 3-16)

Therefore, providing a reference voltage generated across said reference resistor is applied across said at least one current adjustment resistor to generate said at least one internal reference current (col. 5-6, lines 46-60).

Examiner notes, Applicant claims wherein the reference resistor is broadly "connected" between said first and second terminals. The current claim language is distinguishable from the reference resistor being "directly connected" between said first

and second terminals and would better help place the Application in condition for allowance.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hansen et al (5,910,792) brightness control in a Field emission display.

Huang et al (6,501,449) High matching precision OLED driving using a current-cascaded method.

Shimozono et al (2003/0071677) Constant current circuit for controlling variation in output current.

Maede et al (2003/0151374) OELD drive circuit and OLED using the same.

Sase et al (2003/0122808) Display device drive cicuit.

Sakuragi et al (6,222,357) Current output circuit with controlled holdover capacitors.

Shih et al (2005/0030273) Current drive system with high uniformity reference current and in current driver.

Yamaguchi et al (6,332,661) Constant current driving apparatus and constant current driving.

Nishitoba et al (2002/0084812) Driving circuit and constant current driving apparatus using the same.

Dennehey (6,972,742) Method of current balancing in visual devices.

Nagumo et al (6,400,349) Driving circuit and LED head with constant turn-on time.

Holloman (6,097,360) Analog driver for LED or similar display element.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Grant D Sitta/
Examiner, Art Unit 2629
July 15, 2009